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PATENT

Atty. Docket No. 8071-55 (OPP 030490US)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Yi Chung	Examiner: Yevsikov, Victor V.
SERIAL NO.:	10/800,180	Group Art Unit: 2825
FILED:	March 12, 2004	
FOR:	THIN FILM TRANSISTOR ARRAY PANEL AND MANUFACTURING METHOD THEREOF	

Dated: February 3, 2005

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF FORMAL DRAWINGS

Sir:

Applicant submits herewith fourteen (14) sheets of formal drawings depicting FIGS. 1A-8B for this application.

Respectfully submitted,

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CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postpaid in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 3, 2005.

Dated: February 3, 2005

Michael F. Morano